What is Claimed is:

[c1] A method for processing packets in a network, said network including a direct memory access (DMA) device including an input port, a memory unit, a plurality of processors, and an output port, said method comprising:

receiving a packet through the input port;

performing a mapping function which includes assigning said packet based on information contained in said packet; and

sending said packet to one of said plurality of processors based on the assignment performed by said mapping function.

[c2] The method of claim 1, wherein said mapping function assigns a plurality of packets in a manner which causes said processors to process a substantially equal number of packets.

[c3] The method of claim 1, wherein said information includes a predetermined number of bits in at least one header field of said packet.

[c4] The method of claim 3, wherein said header field contains at least one of source identification information and exchange originator identification information for said packet.

[c5] The method of claim 1, wherein said mapping function assigns packets from a same sequence to a same one of said plurality of processors.

[c6] The method of claim 1, wherein said mapping function is a hash function.

[c7] The method of claim 6, further comprising:

storing said packet in the memory unit,

wherein said hash function transforms a key that specifies a set of items into a table address, said key corresponding to at least one header field of said packet, said set of items including a plurality of received packets, and said table address corresponding to a selection of said one of said plurality of processors.

[c8] The method of claim 7, further comprising:

sending pointer information to said one of said plurality of processors, said

pointer information indicating a location of said packet stored in said memory unit.

[c9] The method of claim 6, wherein said hash function is implemented by one of logical and arithmetic instructions, a hardwired circuit, and a table lookup.

[c10] The method of claim 6, wherein said packet is transmitted using a fibre channel protocol, and wherein said header information includes source identification information and exchange originator identification data.

[c11] A device for routing packets in a network, comprising:

an input port for receiving a packet that includes header information;

a plurality of processors;

a memory unit; and

a direct memory access (DMA) device which performs a mapping function that includes assigning said packet based on said header information, and which routes said packet to one of said plurality of processors based on the assignment performed by said mapping function.

[c12] The device of claim 11, wherein said mapping function assigns a plurality of packets in a manner which causes said processors to process a substantially equal number of packets.

[c13] The device of claim 11, wherein said direct memory access device stores said packet in the memory unit.

[c14] The device of claim 11, wherein said direct memory access device sends pointer information to said one of said plurality of processors, said pointer information indicating a location of said packet stored in said memory unit.

[c15]

The device of claim 11, further comprising:

at least one queue,

wherein said direct memory access device stores pointer information in said queue, said pointer information indicating a location where said packet is stored in the memory unit, and

wherein said one of said plurality of processors reads said pointer

information from said queue to access the packet stored in the memory unit.

[c16] The device of claim 15, wherein said queue is a FIFO buffer.

[c17] The device of claim 15, wherein said queue is a ring buffer.